REMARKS

Concurrently filed herewith is a Request for Continued Examination (RCE).

Claims 1-12, 21-24, and 28-35 are all the claims presently being examined in the application. Claims 34-35 have been added to more completely define the invention.

In the Final Office Action dated March 16, 2006, Claims 1-12, 21-24, and 28-33 stand rejected only on prior art grounds, and specifically under 35 U.S.C. § 102(e) as being anticipated by Joshi et al. (U.S. Patent No. 6,921,982), commonly assigned with the present application.

This rejection is respectfully traversed in view of the following discussion.

It is noted that any claim amendments herein are made only for more particularly pointing out the invention, and not necessarily for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

Further, it is noted that, notwithstanding any claim amendments made herein or later during prosecution, Applicant's intent is to encompass equivalents of all claim elements. Thus, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Applicant submits that all of the pending claims are patentable over the prior art of record.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed (e.g., as exemplarily defined in independent claim 1) is directed to a doublet-gate field effect transistor, which includes a strained-silicon channel formed adjacent a source and a drain, a first gate formed over a first side

of the channel, a second gate formed over a second side of the channel, a first gate dielectric formed between the first gate and the strained-silicon channel, and a second gate dielectric formed between the second gate and the strained-silicon channel. The strained-silicon channel is non-planar.

Independent claim 21 recites a somewhat similar combination as claim 1, including "a strained-silicon channel formed adjacent a source and a drain; a first gate formed over a first side of said channel; a second gate formed over a second side of said channel. . . wherein said strained-silicon channel comprises a fin" (emphasis ours).

Independent claim 30 recites a semiconductor device, which includes, inter alia, "a strained-silicon channel formed adjacent a source and a drain; a first gate formed over a first sidewall of said channel; a second gate formed over a second sidewall of said channel..... wherein said strained-silicon channel is non-planar, and said first and second sidewalls are opposing to each other" (emphasis ours).

Independent claim 31 recites a somewhat similar combination, including, inter alia, "a strained-silicon channel formed adjacent a source and a drain, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel..... wherein said strained-silicon channel is non-planar, and is fixed to the substrate by said first and second gates" (emphasis ours).

Such combinations of features are not taught or suggested by any of the piror art of record.

II. THE PRIOR ART REJECTION

Joshi US 6,921,982:

Joshi et al. is fundamentally different from the claimed invention and indeed is irrelevant thereto.

In response to the Examiner's arguments on page 7 of the Office Action, the Examiner acknowledged that the core material 24 is NOT a gate. As such, Joshi teaches (e.g., Figure 4) only one gate 18 that covers the channel 32 on its outer surface. The inner surface is laid on the core material 24 and is not a gate. The structure defined in claim 1 comprises "a first gate formed over a first side of said channel and a second gate formed over a second side of said channel".

That is, both sidewall surfaces of the channels are gated. The Examiner acknowledged that Joshi does not form a double-gate FinFET, as there is no second gate on the inner sidewall to control the channel, but the Examiner asserted that the claims do not recite such a limitation (last paragraph of page 7).

While Applicant respectfully disagrees with the Examiner, to speed prosecution, claims 1 and 21 now clearly recite such a limitation for the Examiner. Thus, there is no teaching or suggestion of the "double-gate field effect transistor" of claims 1 and 21.

Further, as discussed in the previous Amendment (that of November 8, 2005, Amendment), Joshi et al. teaches a FET where the device channel 32 (e.g., see Fig. 4 and Figure 8F which shows a different view of the structure of Figure 4) is formed as a shell (envelope) 32 over a slab (core) 24. The core 24 and the shell (envelope) 32 are semiconductors with different natural lattice constants.

Per Joshi's teaching (Figures 2a and 2b) when the shell 32 is grown epitaxially over the core 24, the shell 32 will attempt to match the core's lattice constant and will form a strained layer (as illustrated by the example of strained silicon over Ge in Fig. 2b). As such, the "channel" 32 can have compressive or tensile strain based on the core 24 material. The FET can have from one to four gates (Figures 8A to 8D, gates labeled as 95 to 98).

The present invention teaches a strained-channel double-gate FinFET, which includes a thin strained-silicon channel 11 (e.g., a non-planar strained-silicon channel as defined by independent claim 1 or a fin as defined in claim 21) (all reference numerals used herein being exemplary and for the Examiner's clarity only and not for limiting the claims), a first gate dielectric 12 and a first gate conductor 13 on one sidewall of the fin, and a second gate dielectric 15 and a second gate conductor 16 on the opposite side of the fin (see Fig. 22 which shows a cross-section of the present invention).

Joshi et al. clearly does not teach or suggest a FinFET structure, let alone a structure as in the invention.

Once again, Joshi does not teach or suggest a FinFET structure, as the structure disclosed by Joshi (e.g. Fig. 4) includes a channel 32 (envelope), and a gate 18 that is formed over the outer sidewall of the envelope 32, while the inner sidewall (28 or 30) of the envelope 32 is in contact with a core material 24. The core material 24 is not a gate.

Joshi's structure does not form a double-gate FinFET since there is no second gate formed on the inner sidewall to control the channel. The gate material is only deposited on the outer surface of the "channel" (i.e., the envelope 32). As a result, the device taught by Joshi is merely a single-gate, non-planar strained-channel FET.

Hence, referring to independent claim 1 (and claim 21 and somewhat similarly in independent claim 31), Joshi does not teach or suggest "*a first gate formed over a first side of said channel and a second gate formed over a second side of said channel*".

Thus, Joshi has the slab wrapped around the core 24 and only one surface of the core is being gated, not two! This structure of Joshi's is clearly distinguished from the claimed invention (see the cross section of Figure 22) which includes "*a first gate (13) formed over a first side of said channel (11) and a second gate (16) formed over a second side of said channel (11)*". Thus, in contrast to Joshi's Figure 4, the invention has a slab (channel) which is sandwiched between two (2) gates. This is not shown in Joshi.

Additionally, with regard to claim 21, the Examiner asserts that Joshi refers to the channel as a fin. However, as clearly illustrated in the figures of Joshi, the channel 32 has an inverted "U" shape. The channel shape does not resemble the FinFET structure defined in the application or that defined by Hu Chenming et al., U.S. Patent No. 6,413,802 entitled "FinFET transistor structures having a double gate channel extending vertically from a substrate and methods of manufacture". As mentioned in the Amendment of November 8, 2005, Chenming et al. discloses the widely accepted definition for a FinFET structure. Claim 21 requires that the channel will be a fin, which is different than the shape of an inverted "U".

Referring to the Examiner's rejection of claim 31 (page 6 of the Office Action):

Claim 31 recites "a strained-silicon channel formed adjacent a source and a drain, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor".

As defined in claim 31, the strain in the channel is introduced by a sacrificial stressor. Since the stressor is sacrificial, it is removed during the process of building the structure, and thus it is not present in the final structure. This is different than the structure taught by Joshi where the core 24, on which the channel 32 is deposited, is present in the final structure. The core being the stressor (as explained in col. 5 and 6 of Joshi et al.) is present in the final structure taught by Joshi.

In the present invention, removing the stressor allows access to the other surface of the channel, and form a gate on that surface. Thus, the device functions as a double-gate FET, where the channel is controlled from both surfaces.

In Response to the Examiner's arguments on page 8 of the Office Action:

Joshi is using relaxed SiGe as a core (Col. 6, lines 9-10): " *the channel core 24 is preferably a compound comprising silicon and germanium that is processed to exhibit a relaxed lattice structure.*" Relaxation of SiGe as described by Joshi requires the formation of dislocations (for a further discussion thereon, the Examiner is referred to the list of cited papers provided by Applicant in the November 8, 2005 Amendment).

Thus, Joshi's assertion that the SiGe is free from dislocation is incorrect. While the patent law as suggested by the Examiner may enable SiGe to relax without forming defects in the process of relaxation, the laws of physics do not and such would not have been recognized by one of ordinary skill in the art.

In view of all of the foregoing, independent claims 1 and 21 (as well as independent claims 30-31) are not taught or suggested by Joshi et al.

Dependent Claims

The dependent claims are similarly allowable based not only on their dependency from their respective independent claims, but also for the additional limitations which they recite, as discussed in the previous Amendment incorporated herein by reference.

Further, new dependent claims 34 and 35 define the "double-gate" operation in further detail. AS mentioned above, Johsi is devoid of such a teaching.

In view of all of the foregoing, Joshi fails to anticipate, or, for that matter, render obvious the claimed subject matter, either alone or in combination with any of the other prior art of record.

III. FORMAL MATTERS AND CONCLUSION

Claim 29 has been amended to overcome the claim objection.

In view of the foregoing, Applicant submits that claims 1-12, 21-24, and 28-35, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

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